IN THE CLAIMS

1 (Currently Amended). A method comprising:

providing a register accessible by a plurality of central processing units; and

indicating whether data in said register is available for a given central processing unit by providing different indicators assigned to each of a plurality of central processing units and enabling the given central processing unit to reset its indicator when the data in said register is no longer useful to the given central processing unit.

2 (Previously Presented). The method of claim 1 including indicating for each of a plurality of central processing units whether the data is available for a given central processing unit.

3 (Previously Presented). The method of claim 2 including requiring a central processing unit to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers.

4 (Previously Presented). The method of claim 3 including providing a bit for each item of data indicating whether a given central processing unit can access that data.

5 (Previously Presented). The method of claim 4 including resetting said bit when said data is accessed by a given central processing unit.

6 (Currently Amended). The method of claim 1 ~~5~~ including ~~providing a register with a bit for each of a plurality of central processing units, enabling a central processing unit to reset said bit when the data is no longer useful to the central processing unit, and~~ preventing any central processing unit from writing data to said register until all of the ~~bits~~ indicators for the plurality of central processing units indicate that the data is no longer useful to any other central processing unit.

7 (Previously Presented). The method of claim 6 including indicating the central processing unit which will utilize the data written into the register.

8 (Previously Presented). The method of claim 1 includes enabling a plurality of central processing units to access a register at the same time.

9 (Previously Presented). The method of claim 1 including providing specialized central processing units for mathematical operations and for memory.

10 (Previously Presented). The method of claim 1 including providing an input central processing unit, an output central processing unit and coupling said input, output and specialized central processing units to said register through a cross-bar connection.

11 (Currently Amended). A computer readable ~~An article comprising a~~ medium storing instructions that, if executed, enable a processor-based system to:

make a register accessible by a plurality of central processing units in said system; ~~and~~

provide different indictors for each of a plurality of central processing units;

indicate whether data in said register is available for a given processing unit; and

enable the given central processing unit to reset its indicator when data in the register is no longer useful for the given central processing unit.

12 (Currently Amended). The medium ~~article~~ of claim 11 further storing instructions that enable the processor-based system to determine whether data is available in a register for a particular processing unit.

13 (Currently Amended). The medium ~~article~~ of claim 12 further storing instructions that enable the processor-based system to prevent execution of an instruction until the data needed to execute the instruction is available in one or more registers.

14 (Currently Amended). The medium ~~article~~ of claim 13 further storing instructions that enable the processor-based system to check a bit in said register for each item of data indicating whether a processing unit can access said data.

15 (Currently Amended). The medium ~~article~~ of claim 14 further storing instructions that enable the processor-based system to reset said bit when said data is accessed by a processing unit.

16 (Currently Amended). The medium ~~article~~ of claim 15 further storing instructions that enable the processor-based system ~~to identify in said register a bit for a processing unit from among bits for a plurality of processing units, reset said bit when the data is no longer useful to a processing unit, and~~ to avoid writing said data to said register until all the bits indicate that the data is no longer useful to any other processing unit.

17 (Currently Amended). The medium ~~article~~ of claim 16 further storing instructions that enable the processor-based system to indicate which processing unit will utilize the data written into the register by another processing unit.

18 (Currently Amended). A digital signal processor including:

a plurality of central processing units; and

a first register coupled to said plurality of central processing units, said register including a plurality of general purpose second registers each accessible by said plurality of processing units, at least one of said second registers indicating whether data in said first register is available for a given one of said plurality of central processing units.

19 (Previously Presented). The processor of claim 18 wherein said processing units are coupled to said register by a cross-bar connection.

20 (Previously Presented). The processor of claim 18 including a plurality of registers each including a bit indicating for each of said processing units whether the data in the general purpose register is available for a given processing unit.

21 (Previously Presented). The processor of claim 18 wherein a processing unit must wait to execute an instruction until the data it needs to execute the instruction is available in one or more general purpose registers.

22 (Previously Presented). The processor of claim 21 wherein each processing unit has a designated bit for each general purpose register indicating whether a given processing unit can access the data.

23 (Previously Presented). The processor of claim 18 wherein none of the processing units can write data to a general purpose register until all of the bits indicate that the data is no longer useful to any other processing unit.

24 (Previously Presented). The processor of claim 18 including a plurality of general purpose registers, each of said general purpose registers including a data section and a storage area for a bit for each of said plurality of processing units.

25 (Previously Presented). The processor of claim 18 wherein said general purpose register is accessible by each of said processing units at the same time.

26 (Previously Presented). The processor of claim 18 wherein at least one of said processing units is an input processing unit and another of said processing unit an output processing unit.

27 (Previously Presented). The processor of claim 26 further including at least one multiply and accumulate processing unit.

28 (Original). The processor of claim 27 including at least one processing element for storing data in a random access memory.

29 (Original). The processor of claim 18 wherein no master processing element is included and instead, the sequence of operations in said digital signal processor is driven by the availability in a general purpose register of data needed to execute instructions.

30 (Previously Presented). The processor of claim 18 including a plurality of special purpose processing units that may each access a register at the same time.